FIG . 1
Related Art

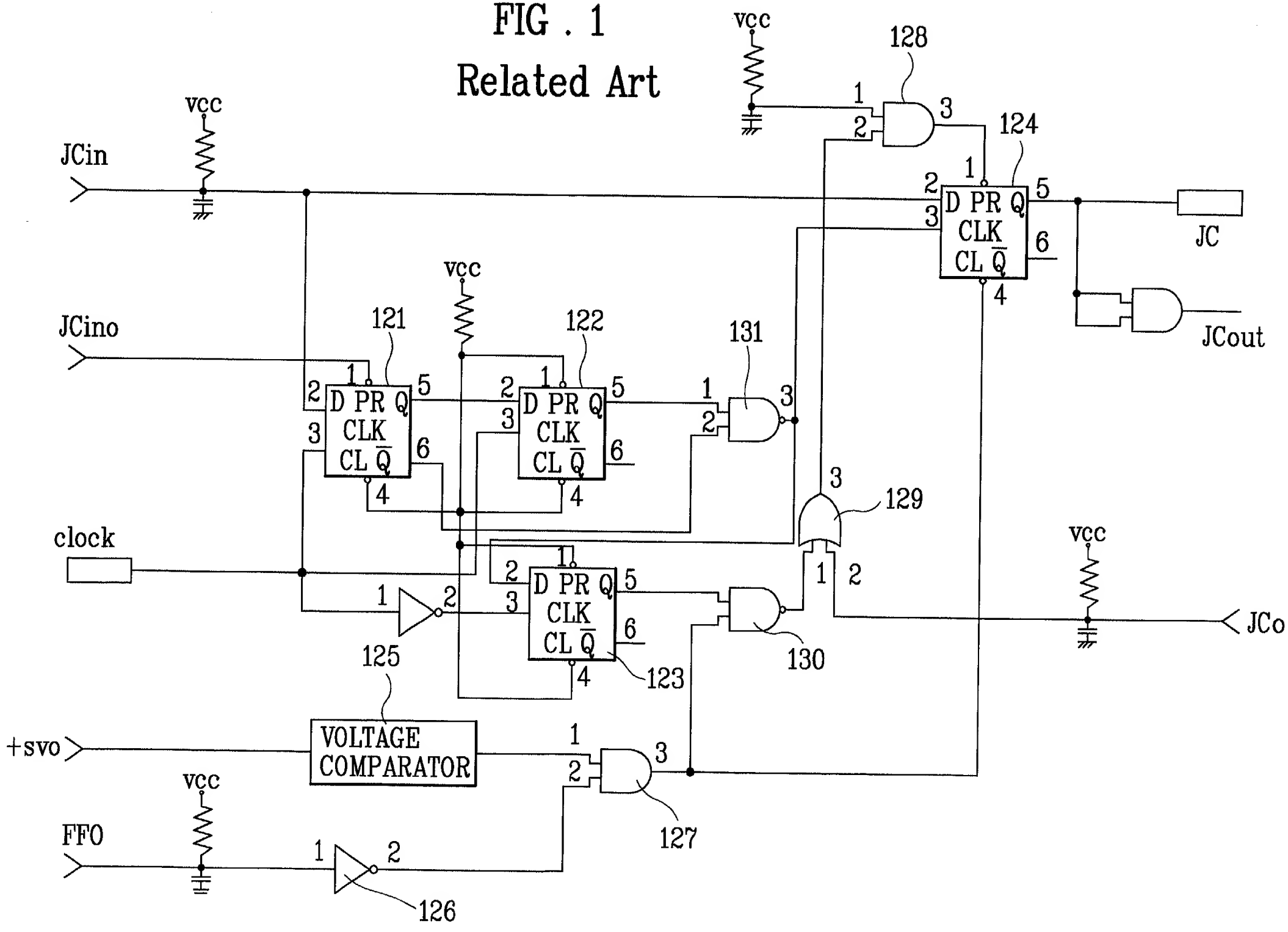

FIG . 2
Related Art

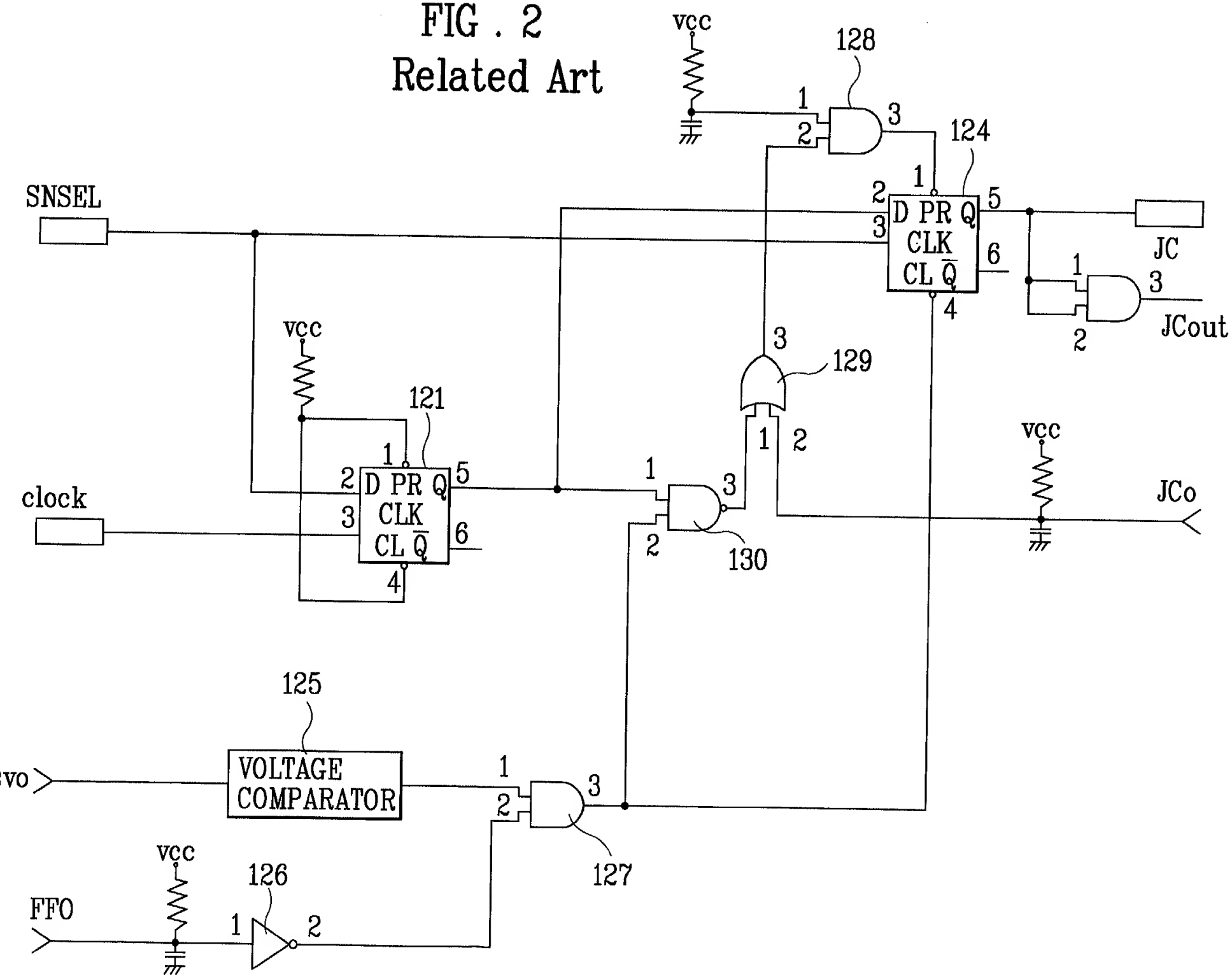

FIG. 3

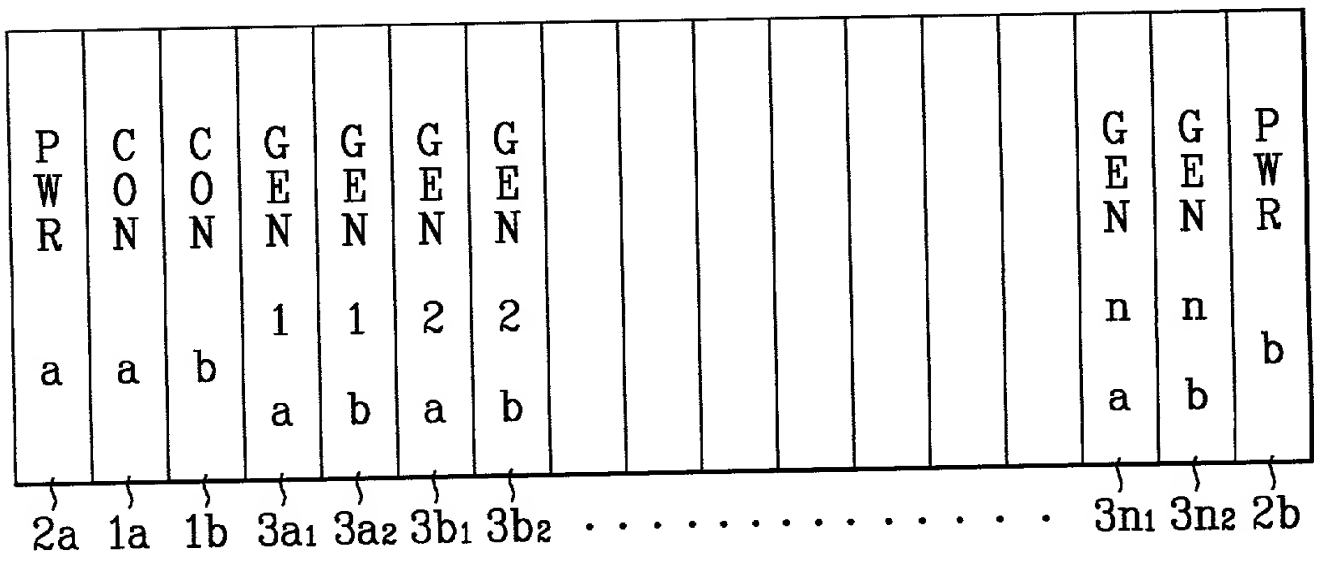
PWR a
CON a
CON b
GEN 1 a
GEN 1 b
GEN 2 a
GEN 2 b
GEN n a
GEN n b
PWR b
2a
1a
1b
3a1
3a2
3b1
3b2
3n1
3n2
2b

FIG. 4

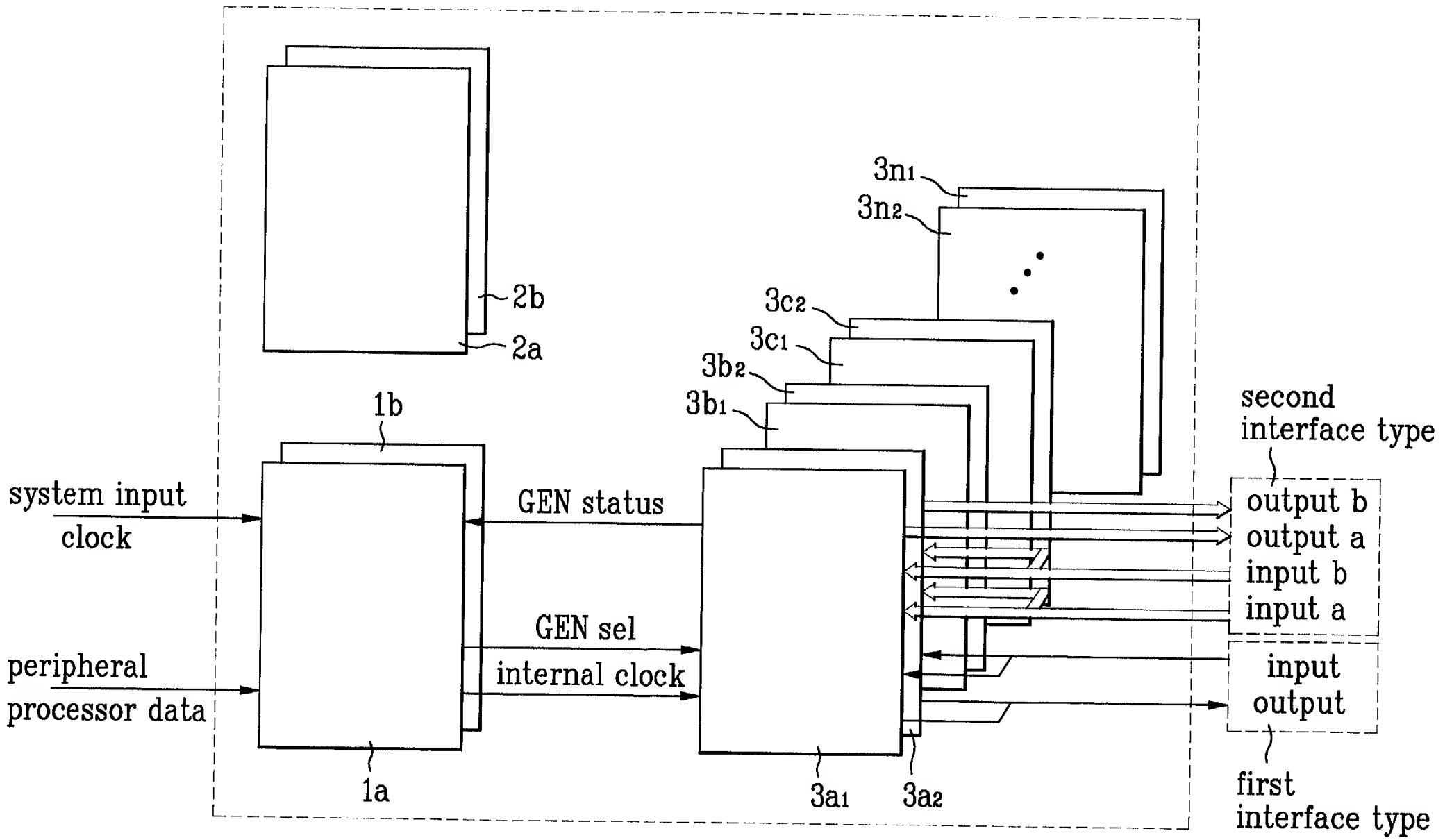
2b
2a
1b
3n1
3n2
3c2
3c1
3b2
3b1
second
interface type
system input
clock
GEN status
output b
output a
input b
input a
GEN sel
internal clock
peripheral
processor data
input
output
1a
3a1
3a2
first
interface type

FIG. 5

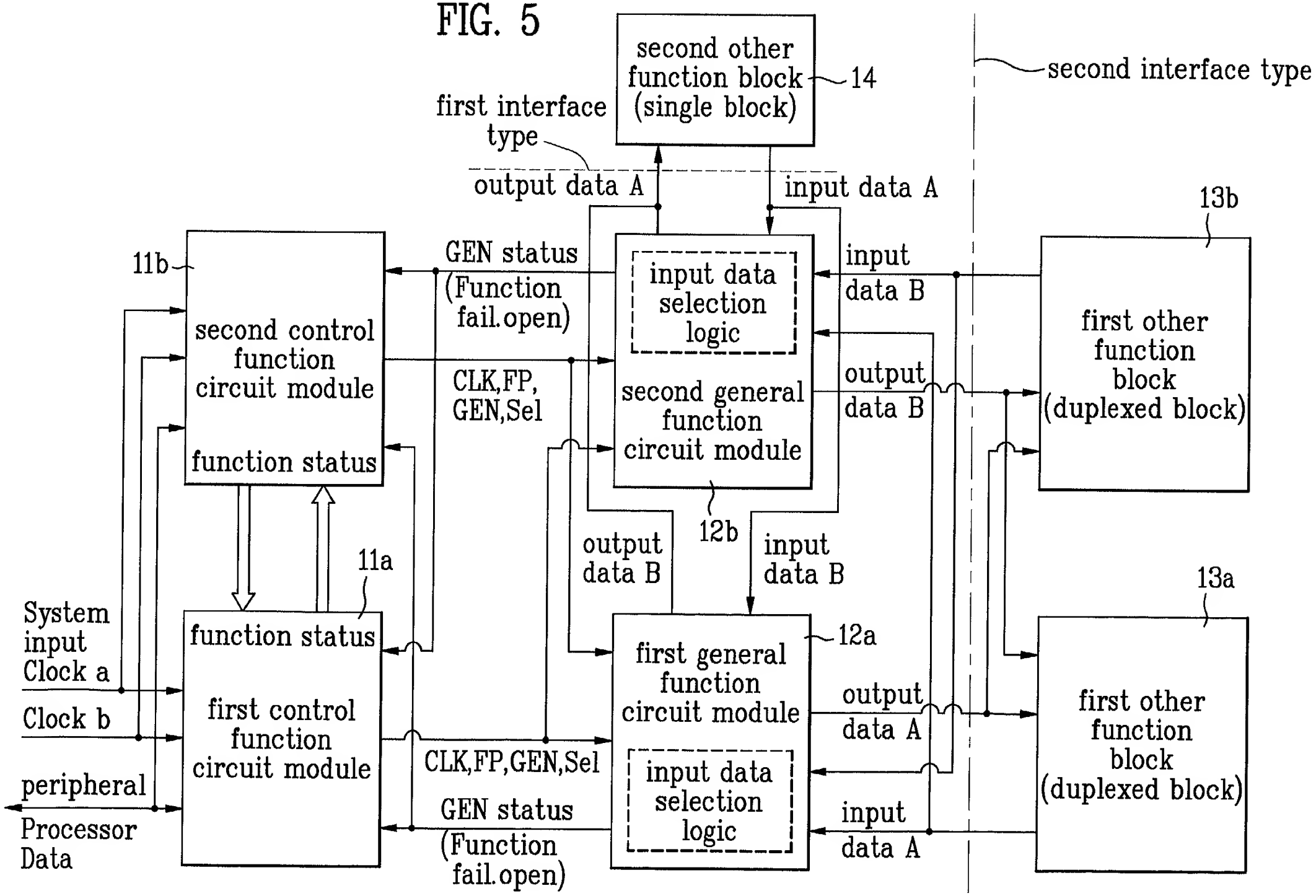
second other function block (single block)
14
second interface type
first interface type
output data A
input data A
13b
11b
GEN status (Function fail.open)
input data selection logic
input data B
second control function circuit module
CLK,FP, GEN,Sel
second general function circuit module
output data B
first other function block (duplexed block)
function status
12b
output data B
input data B
11a
13a
System input Clock a
function status
first general function circuit module
12a
output data A
Clock b
first control function circuit module
input data selection logic
first other function block (duplexed block)
CLK,FP,GEN,Sel
peripheral
GEN status (Function fail.open)
input data A
Processor Data

FIG. 6A

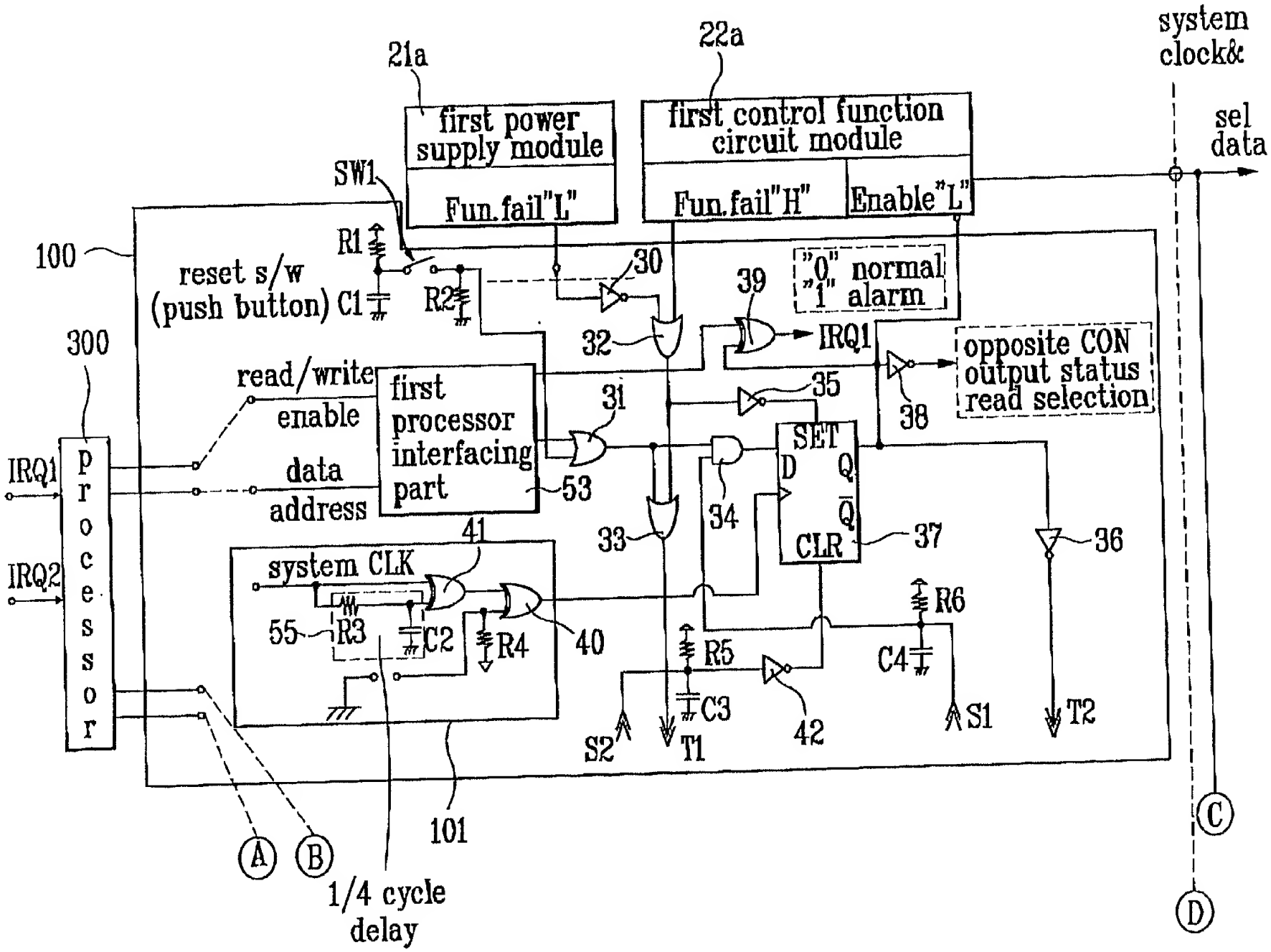
21a
22a
system clock&
first power supply module
Fun.fail"L"
first control function circuit module
Fun.fail"H"
Enable"L"
sel data
SW1
R1
100
reset s/w (push button)
C1
R2
30
39
"0" normal "1" alarm
32
IRQ1
opposite CON output status read selection
300
read/write enable
data address
first processor interfacing part
53
31
35
38
SET
D
Q
CLR
37
34
33
36
IRQ1
IRQ2
processor
41
system CLK
55
R3
C2
R4
40
R5
C3
R6
C4
S1
T2
S2
T1
42
101
A
B
1/4 cycle delay
C
D

FIG. 6B

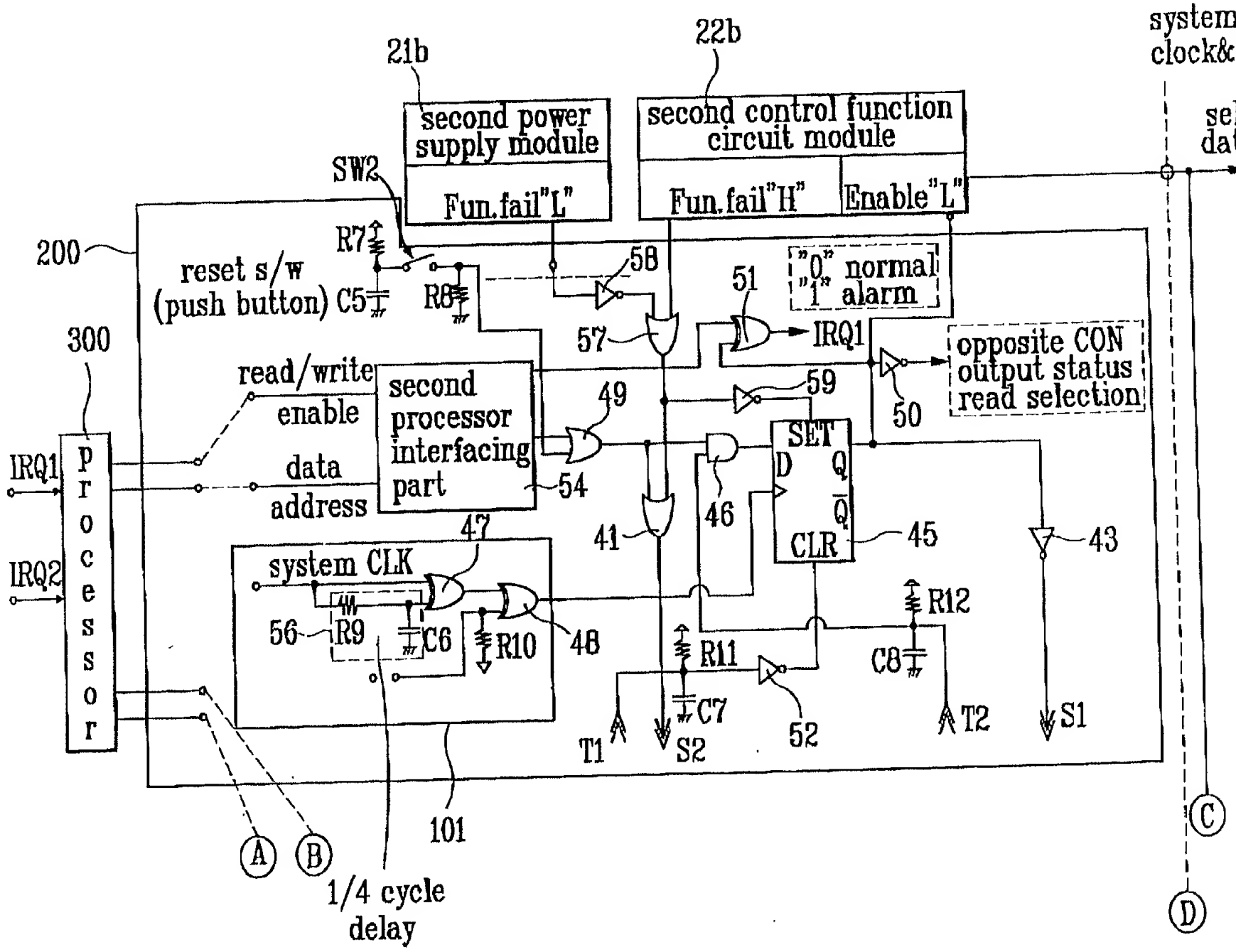
21b
second power supply module
Fun.fail"L"
22b
second control function circuit module
Fun.fail"H"
Enable"L"
system clock&
sel data
SW2
200
R7
reset s/w (push button)
C5
R8
58
51
"0" normal
"1" alarm
57
IRQ1
300
read/write
enable
data
address
second processor interfacing part
54
49
59
50
opposite CON output status read selection
SET
D
Q
CLR
45
46
41
43
IRQ1
IRQ2
processor
47
system CLK
56
R9
C6
R10
48
R11
C7
R12
C8
T1
S2
52
T2
S1
101
A
B
1/4 cycle delay
C
D

FIG. 7

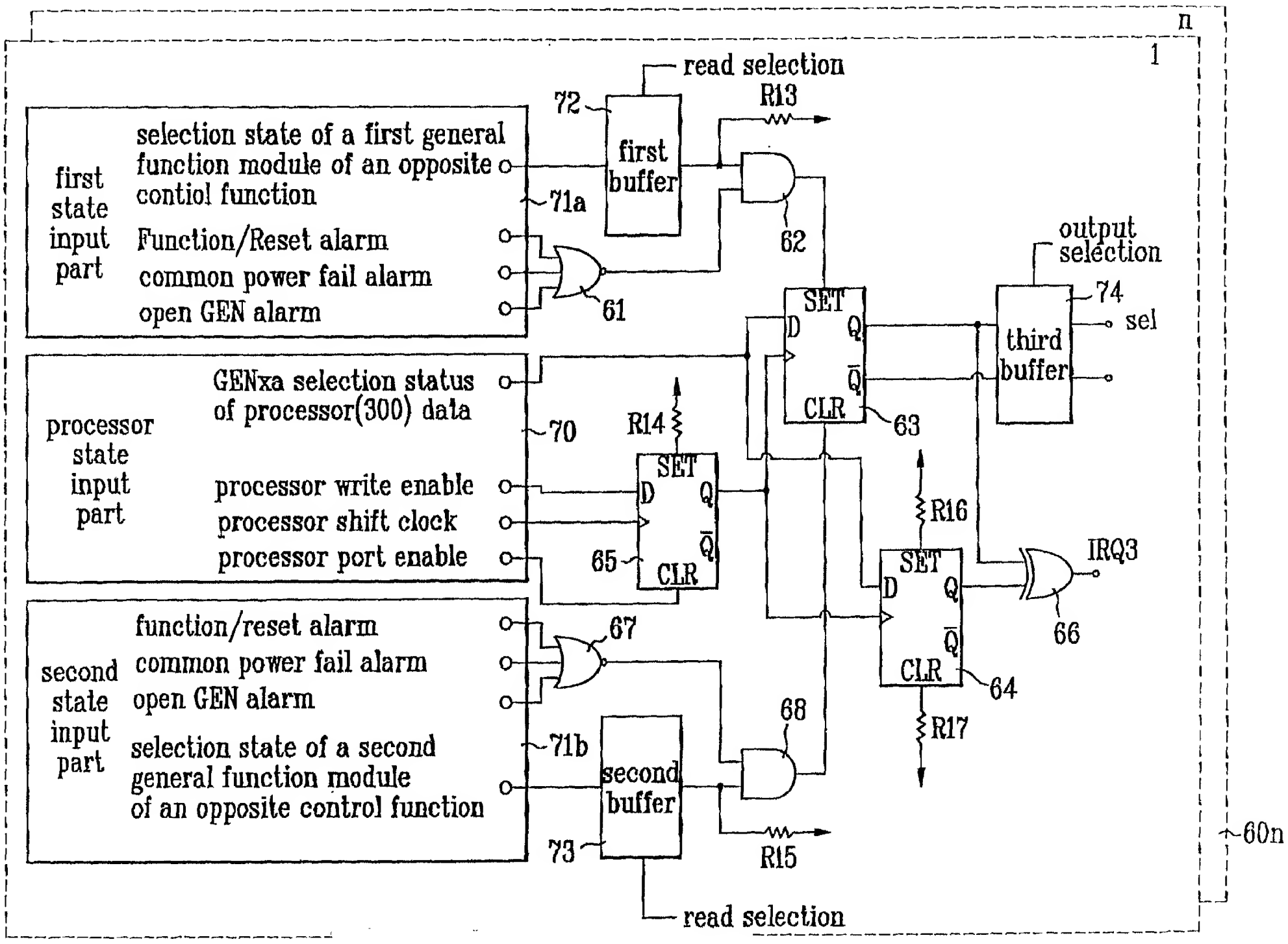
n
1
read selection
R13
72
first buffer
first state input part
selection state of a first general function module of an opposite contiol function
Function/Reset alarm
common power fail alarm
open GEN alarm
71a
61
62
output selection
74
sel
third buffer
SET
D
Q
CLR
63
processor state input part
GENxa selection status of processor(300) data
processor write enable
processor shift clock
processor port enable
70
R14
65
R16
IRQ3
66
64
R17
second state input part
function/reset alarm
common power fail alarm
open GEN alarm
selection state of a second general function module of an opposite control function
71b
67
68
second buffer
73
R15
60n
read selection

FIG . 8